IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Yeshwanth Narendar et al.		
Title:	METHOD FOR TREATING SEMICONDUCTOR PROCESSING COMPONENTS AND COMPONENTS FORMED THEREBY		
App. No.:	10/824,329	Filed:	April 14, 2004
Examiner:	Julio J. Maldonado	Group Art Unit:	2823
Customer No.:	34456	Confirmation No.:	5396
Atty. Dkt. No.:	1035-E4371		

MS AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

REQUEST FOR RECONSIDERATION

Dear Sir:

In response to the Office Action mailed April 20, 2007, please reconsider the positions stated in the current Office Action for the following reasons.

Claims 1, 4-11 and 14-21 are pending herein.

1. Claims 1, 4-9, 14-19 and 21 were rejected under §103 over Thilderkvist et al. in view of Kumar et al. This rejection is respectfully traversed for the following reasons.

The claimed invention is drawn to a semiconductor processing component comprising SiC, having an outer surface portion that consists essentially of CVD-SiC. That outer surface portion has a surface impurity level of not greater than two times (2X) the bulk impurity level, which is measured at a depth of at least microns from the outer surface. This notably reduced surface impurity level may be achieved through processing as described in the present specification, namely a substractive process relying on repeated oxidation and etching steps to

CERTIFICATE OF TRANSMISSION/MAILING
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents on 10/22/07

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